REMARKS

Claims 1-20 were pending in the present application. Claims 1 and 11 have been amended. Accordingly, claims 1-20 remain pending in the application.

The Examiner has objected to the Title as being to broad. The Applicant has changed the title to be more descriptive of the invention.

Claims 1-20 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of Gulick et al. (U.S. Patent No. 6,697,890). The Applicant has filed herewith a timely filed Terminal Disclaimer in accordance with 37 C.F.R. 1.321(c).

Claims 1-8 and 11-18 stand rejected under 35 U.S.C. 102(b) as being anticipated by Roach et al. (U.S. Patent No. 6,005,849) (hereinafter 'Roach'). The Applicant respectfully traverse this rejection.

Claims 9, 10, 19, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Roach in view of Avery (U.S. Patent No. 6,691,185). The Applicant respectfully traverse this rejection.

The Applicant's claim 1 recites

"An input/output node for a computer system comprising:

a first receiver unit configured to receive a first command from a first node on a first communication path;

a first transmitter unit coupled to transmit a first corresponding command that corresponds to said first command to a second node on a second communication path;

a second receiver unit configured to receive a second command on a third communication path;

a second transmitter unit coupled to transmit a second corresponding command that corresponds to said second command to said first node on a fourth communication path; and

a bridge unit coupled to receive selected commands from said first receiver and said second receiver and configured to transmit commands corresponding to said selected commands upon a peripheral bus." (Emphasis added)

The Examiner has asserted that Roach teaches each and every claim element recited in claim 1 and claim 11. However, in the Examiner's rejection, the Examiner merely states "As per claim 1, the reference of roach et al. teaches "first and second receiver units" in Fig. 3, element 30 and Fig. 5B; "first and second transmitter units" in Fig. 3, element 32 and Fig 5A and "a bridge unit" in Fig. 3, element 22 and col. 4, lines 57-65."

Roach discloses at col. 4, lines 53-65

> "Unlike conventional protocol engines, the full-duplex communication processor 22 does not include a microprocessor. Instead, dual microcoded engines are employed in order to separate the protocol engine receive tasks from the protocol engine transmit tasks. In particular, the full-duplex communication processor 22 includes a receive protocol engine 30 and a transmit protocol engine 32. These protocol engines communicate to each other through a transfer ready queue 60. The receive protocol engine 30 validates the receive frame headers received from the receive frame buffer 28. The transmit protocol engine 32 builds transmit frames and sends them to the Fibre Channel data link 24 through a transmit FIFO 66 and the NL port 36.
> The full duplex communication processor 22 works in conjunction with a host computer 40 that includes host..." (Emphasis added)

Roach also discloses at col. 5, lines 18-20 "FIG. 5 shows additional details of the full-duplex communication processor 22 of a preferred embodiment of the invention." (Emphasis added)

The Applicant finds it difficult to discern, from the Examiner's assertion, how Roach teaches the Applicant's invention. Specifically, the Examiner cites that in Roach

element 30 and Fig. 5B are a first and second receive unit. The Applicant asserts that as illustrated in Fig. 5B, Fig. 5B is simply a more detailed diagram of element 30. Thus, **they are the same element and so cannot be a first and second receiver unit.** The Examiner also asserts that in Roach the first and second transmitter units are element 32 of Fig. 3 and Fig 5A. Again, the Applicant asserts that as illustrated in Fig. 5A, Fig. 5A is simply a more detailed diagram of element 32. Thus, **they are the same element and so cannot be a first and second transmitter unit.** Further, the Examiner also cites that element 22 is a bridge unit. However, element 30 and 32 are part of element 22 and not separate elements as required by claim 1.

From the foregoing, it is clear that Roach **does not teach or disclose** an I/O node including "a first receiver unit configured to receive a first command from a first node on a first communication path; a first transmitter unit coupled to transmit a first corresponding command that corresponds to said first command to a second node on a second communication path; a second receiver unit configured to receive a second command from said second node on a third communication path; a second transmitter unit coupled to transmit a second corresponding command that corresponds to said second command to said first node on a fourth communication path; a bridge unit coupled to receive selected commands from said first receiver and said second receiver ..."

Avery is directed toward an apparatus for merging a plurality of data streams into a single data stream. The Applicant submits that Avery does not teach or disclose an I/O node including "a first receiver unit configured to receive a first command from a first node on a first communication path; a first transmitter unit coupled to transmit a first corresponding command that corresponds to said first command to a second node on a second communication path; a second receiver unit configured to receive a second command from said second node on a third communication path; a second transmitter unit coupled to transmit a second corresponding command that corresponds to said second command to said first node on a fourth communication path; a bridge unit coupled to receive selected commands from said first receiver and said second receiver ..."

Accordingly, Applicant believes that claim 1, along with its dependent claims, patentably distinguishes over Roach and over roach in view of Avery for the reasons given above.

Applicant's claim 11 recites

"A computer system comprising:

one or more processors;

one or more input/output nodes connected together and to a given one of said one or more processors **serially in a chain**, each of said input/output nodes including:

a first receiver unit configured to receive a first command from said given one of said one or more processors on a first communication path;

a first transmitter unit coupled to transmit a first corresponding command that corresponds to said first command to a next one of said one or more input/output nodes in said chain on a second communication path;

a second receiver unit configured to receive a second command from said next one of said one or more input/output nodes in said chain on a third communication path;

a second transmitter unit coupled to transmit a second corresponding command that corresponds to said second command to said given one of said one or more processors on a fourth communication path; and

a bridge unit coupled to receive selected commands from said first receiver and said second receiver and configured to transmit commands corresponding to said selected commands upon a peripheral bus." (Emphasis added)

The Applicant's submits that Roach **does not teach or disclose** the features recited in Applicant's claim 11. Likewise, Avery does not teach or disclose the features

recited in Applicant's claim 11. Thus, the Applicant believes that claim 11, along with its dependent claims, patentably distinguishes over Roach and over Roach in view of Avery for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-71700/SJC.

Respectfully submitted,

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